Applicant: Hidetoshi Nishikawa Attorney's Docket No.: 19415-005US1 / PCT-04R-Serial No.: 10/561,552 155/US

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Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

(Previously Presented) A semiconductor integrated circuit device comprising an
output buffer circuit composed of a logic gate that receives data and a driver transistor that
receives, at a control electrode thereof, an output from the logic gate and that is driven according
to the output from the logic gate,

wherein an output control signal that controls an output operation of the driver transistor is inputted to the logic gate;

wherein the logic gate includes

a resistance value switching transistor that receives a selection control signal that varies magnitude of a composite resistance of an on-state resistance of a transistor constituting the logic gate, and that can be switched on/off by the selection control signal,

a first transistor that receives the output control signal at a control electrode thereof and a direct-current voltage at a first electrode thereof;

a switch that is switched on/off by the output control signal and that electrically connects/disconnects a second electrode of the first transistor and the control electrode of the driver transistor; and

the resistance value switching transistor receiving the direct-current voltage at a first electrode thereof, having a second electrode connected to a node at which the second electrode of the first transistor and the switch are connected, and having an on-state resistance lower than the on-state resistance of the first transistor.

wherein the resistance value switching transistor is switched on/off by the selection control signal to switch a rate of change of an output of the driver output transistor. Applicant: Hidetoshi Nishikawa Attorney's Docket No.: 19415-005US1 / PCT-04R-Serial No.: 10/561,552 155/US

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2. (Canceled)

 (Previously Presented) The semiconductor integrated circuit device according to claim 1,

wherein, when an operation frequency of the output buffer circuit is high, the resistance value switching transistor is turned on, and

wherein, when the operation frequency of the output buffer circuit is low, the resistance value switching transistor is turned off.

 (Previously Presented) The semiconductor integrated circuit device according to claim 1,

wherein the first transistor and the resistance value switching transistor are MOS transistors, and

wherein a gate width of the first transistor is made narrower than a gate width of the resistance value switching transistor, or a gate length of the first transistor is made longer than a gate length of the resistance value switching transistor.

 (Previously Presented) The semiconductor integrated circuit device according to claim 1,

wherein an output value determination signal that determines an output from the driver transistor is inputted to the logic gate and the output control signal disables/enables the output operation of the driver transistor,

wherein the logic gate includes

the first transistor, the switch, and the resistance value switching transistor that use the direct-current voltage as a power supply voltage,

the first transistor, the switch, and the resistance value switching transistor that use the direct-current voltage as a ground voltage, and

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a selection switch that selects among outputs from the switch on a side of a power supply voltage and from the switch on a side of a ground voltage according to a value of the output value determination signal, and outputs the selected output to the control electrode of the driver transistor.

 (Original) The semiconductor integrated circuit device according to claim 5, wherein the first transistor and the resistance value switching transistor which are on a side of the power supply voltage are P channel MOS transistors, and

wherein the first transistor and the resistance value switching transistor which are on a side of the ground voltage are N channel MOS transistors.

 (Previously Presented) The semiconductor integrated circuit device according to claim 1,

wherein the switch is a second transistor receiving the output control signal at a control electrode thereof, having a first electrode connected to the second electrode of the first transistor, and having a second electrode connected to the control electrode of the driver transistor.

 (Original) The semiconductor integrated circuit device according to claim 1, wherein the logic gate includes

a plurality of first transistors that have control electrodes serving as an input and that are connected in series between the direct-current voltage and the output of the logic gate, and

a plurality of said resistance value switching transistor receiving at first electrodes thereof the direct-current voltage applied thereto, having second electrodes connected to respective second electrodes of the first transistors, and having an on-state resistance lower than an on-state resistance of the first transistors.

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to the output from the logic gate,

9. (Currently Amended) A semiconductor integrated circuit device comprising an output buffer circuit composed of a logic gate that receives data and a driver transistor that receives, at a control electrode thereof, an output from the logic gate and that is driven according

wherein there [[are]] is provided, within the output buffer circuit, a plurality of transistor switchhes transistor switch having a plurality of transistors that have different on-state resistances and that are connected in parallel between the output of the logic gate and the control electrode of the driver transistor, and

wherein one of the plurality of <u>transistors</u> transistors switches is turned on to switch a rate of change of an output of the driver output transistor.

 (Currently Amended) The semiconductor integrated circuit device according to claim 9,

wherein, when the transistor <u>switch is switches are</u> composed of a first transistor switch and a second transistor switch and an on-state resistance of the first transistor switch is higher than an on-state resistance of the second transistor switch,

if an operation frequency of the output buffer circuit is low, the first transistor switch is turned on and the second transistor switch is turned off, and

if the operation frequency of the output buffer circuit is high, the first transistor switch is turned off and the second transistor switch is turned on.

- 11. (Original) The semiconductor integrated circuit device according to claim 9, wherein, by making MOS transistors constituting each transistor switch have different gate widths and different gate lengths, the transistor switches are made to have different on-state resistances.
- $12. \qquad \hbox{(Previously Presented) The semiconductor integrated circuit device according to claim 1,}$

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wherein there are provided a plurality of said output buffer circuit.

 (Previously Presented) The semiconductor integrated circuit device according to claim 1.

wherein a drive current of the driver transistor is fed to a resistance connected, at one end thereof, to the driver transistor of the output buffer circuit and receiving, at an other end thereof, a direct-current voltage applied thereto.

 (Previously Presented) The semiconductor integrated circuit device according to claim 1.

wherein, by causing a drive current of the driver transistor to flow through a lightemitting device connected, at one end thereof, to the driver transistor of the output buffer circuit and receiving, at an other end thereof, a direct-current voltage applied thereto, the light-emitting device is made to emit light.

15. (Original) A print head comprising:

the semiconductor integrated circuit device of claim 12; and

a plurality of resistances that are each connected, at one end thereof, to the driver transistor of the plurality of said output buffer circuit provided in the semiconductor integrated circuit device and receiving, at an other end thereof, a direct-current voltage applied thereto, and

wherein a drive current of the drive transistor flows through the resistances, and the resistances produce heat.

16. (Original) A print head comprising:

the semiconductor integrated circuit of claim 12: and

a plurality of light-emitting devices that are each connected, at one end thereof, to the driver transistor of the plurality of said output buffer circuit provided in the semiconductor Applicant : Hidetoshi Nishikawa Attorney's Docket No.: 19415-005US1 / PCT-04R-Serial No.: 10/561,552 155/US

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integrated circuit and receiving, at an other end thereof, a direct-current voltage applied thereto, and

wherein a drive current of the driver transistor flows through the light-emitting devices, and the light-emitting devices emit light.

- (Previously Presented) The semiconductor integrated circuit device according to claim 1, wherein the direct-current voltage is a ground voltage.
- 18. (Currently Amended) A semiconductor integrated circuit device comprising an output buffer circuit composed of a logic gate that receives data and a driver transistor that receives, at a control electrode thereof, an output from the logic gate and that is driven according to the output from the logic gate,

wherein there [[are]] is provided, within the output buffer circuit, a transistor switch having a plurality of transistors plurality of transistors switches that have different on-state resistances and that are connected in parallel between the output of the logic gate and the control electrode of the driver transistor, and

wherein one of the plurality of <u>transistors transistors switches</u> is turned on to switch a rate of change of an output of the driver output transistor,

wherein, when the transistor <u>switch is switches are</u> composed of a first transistor switch and a second transistor switch and an on-state resistance of the first transistor switch is higher than an on-state resistance of the second transistor switch,

if an operation frequency of the output buffer circuit is low, the first transistor switch is turned on and the second transistor switch is turned off, and

if the operation frequency of the output buffer circuit is high, the first transistor switch is turned off and the second transistor switch is turned on.